

# DATA SHEET

## **TDA8793**

**8-bit, low-power, 3 V, 100 Msps  
Analog-to-Digital Converter (ADC)**

Product specification  
Supersedes data of 1999 Oct 06  
File under Integrated Circuits, IC02

2000 Nov 20

## 8-bit, low-power, 3 V, 100 Msps Analog-to-Digital Converter (ADC)

## TDA8793

### FEATURES

- 8-bit low-power ADC: 180 mW (typical value)
- 2.7 to 3.6 V operation
- Track-and-hold circuit
- In track-and-hold mode: sampling rate from 70 to 100 Msps
- In non track-and-hold mode: sampling rate from 1 sps to 100 Msps
- CMOS/TTL compatible digital inputs and outputs
- Internal reference voltages
- Adjustable full-scale range possibility with external reference
- Power-down mode: 5 mW.

### APPLICATIONS

- Radio communications
- Digital data storage read channels
- Medical imaging
- Digital instrumentation.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CCA}$	analog supply voltage		2.7	3.0	3.6	V
$V_{CCD}$	digital supply voltage		2.7	3.0	3.6	V
$V_{CCO}$	output stages supply voltage		2.7	3.0	3.6	V
$I_{CCA}$	analog supply current	operating	32	40	48	mA
		standby	0	2	100	$\mu$ A
$I_{CCD}$	digital supply current	operating	12	16	24	mA
		standby	0	0.66	1.1	mA
$I_{CCO}$	output stages supply current	ramp input	–	4	6.5	mA
INL	integral non-linearity	ramp input; $f_{CLK} = 2$ MHz; $V_{CCA} = V_{CCD} = 3$ V	–	$\pm 0.85$	$\pm 1.70$	LSB
DNL	differential non-linearity	ramp input; $f_{CLK} = 2$ MHz; $V_{CCA} = V_{CCD} = 3$ V	–	$\pm 0.25$	$\pm 0.80$	LSB
$f_{CLK(max)}$	maximum clock input frequency		100	–	–	MHz
$P_{tot}$	total power dissipation	$V_{CC} = 3$ V	–	180	–	mW

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8793HL	LQFP32	plastic low profile quad flat package; 32 leads; body $5 \times 5 \times 1.4$ mm	SOT401-1

8-bit, low-power, 3 V, 100 Msp/s  
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BLOCK DIAGRAM

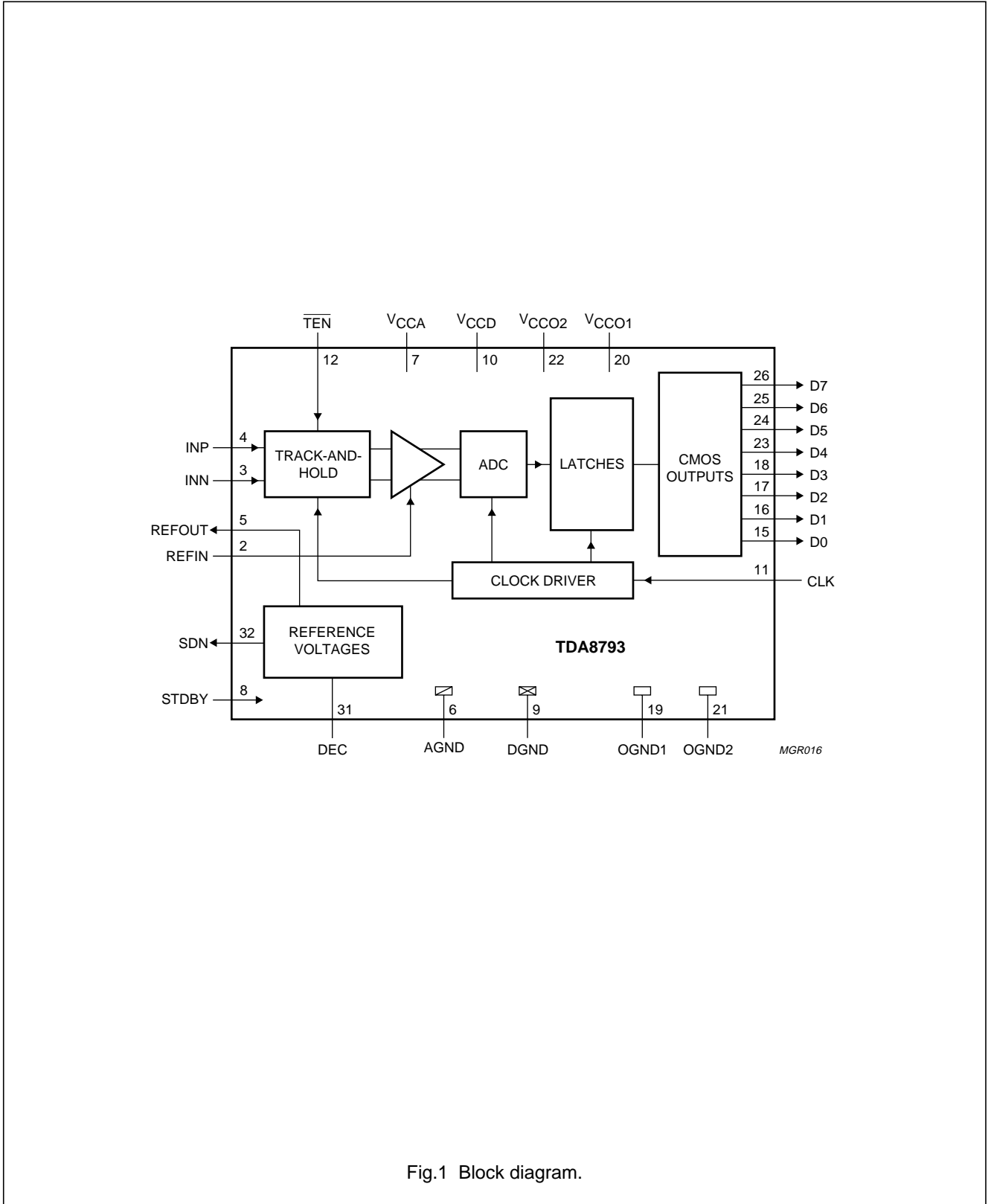


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
REFIN	2	reference input for ADC
INN	3	negative input
INP	4	positive input
REFOUT	5	reference output for AC coupling of input
AGND	6	analog ground
V <sub>CCA</sub>	7	analog supply voltage
STDBY	8	standby mode input
DGND	9	digital ground
V <sub>CCD</sub>	10	digital supply voltage
CLK	11	clock input
TEN	12	track enable input (active LOW)
n.c.	13	not connected
n.c.	14	not connected
D0	15	data output bit 0 (LSB)
D1	16	data output bit 1

SYMBOL	PIN	DESCRIPTION
D2	17	data output bit 2
D3	18	data output bit 3
OGND1	19	output ground 1
V <sub>CCO1</sub>	20	output supply voltage 1
OGND2	21	output ground 2
V <sub>CCO2</sub>	22	output supply voltage 2
D4	23	data output bit 4
D5	24	data output bit 5
D6	25	data output bit 6
D7	26	data output bit 7 (MSB)
n.c.	27	not connected
n.c.	28	not connected
n.c.	29	not connected
n.c.	30	not connected
DEC	31	decoupling
SDN	32	stabilized decoupling node output

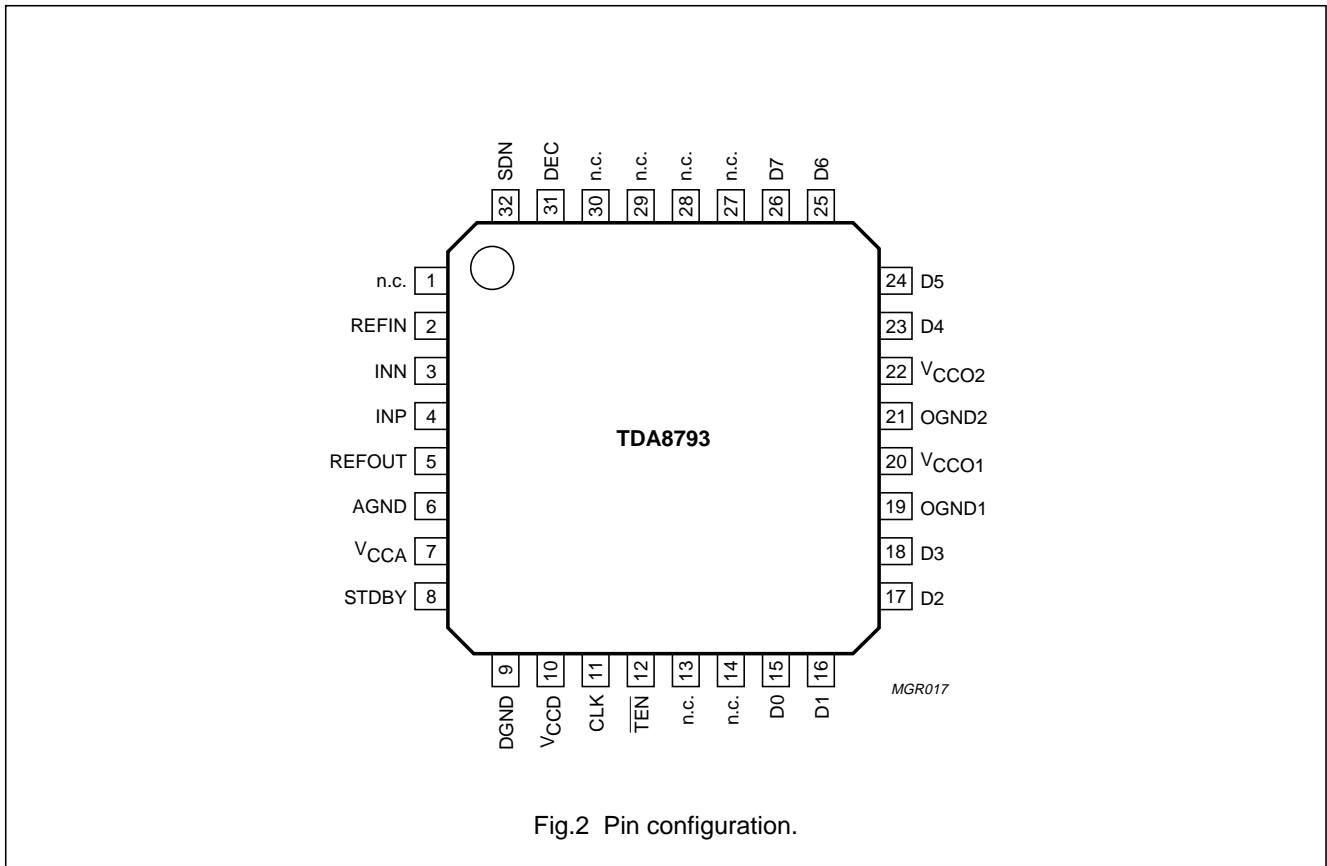


Fig.2 Pin configuration.

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CCA}$	analog supply voltage	note 1	-0.3	+5.0	V
$V_{CCD}$	digital supply voltage	note 1	-0.3	+5.0	V
$V_{CCO}$	output stages supply voltage	note 1	-0.3	+5.0	V
$\Delta V_{CC}$	supply voltage differences between $V_{CCA}$ and $V_{CCD}$		-1.0	+1.0	V
	$V_{CCO}$ and $V_{CCD}$		-1.0	+1.0	V
	$V_{CCA}$ and $V_{CCO}$		-1.0	+1.0	V
$V_n$	voltage on pins INP, INN, CLK, $\overline{TEN}$ and STDBY	note 2	-0.3	+4.5	V
	REFIN		-0.3	+4.5	V
$I_O$	output current		-	10	mA
$T_{stg}$	storage temperature		-55	+150	°C
$T_{amb}$	ambient temperature		0	70	°C

## Notes

1. The supply voltages  $V_{CCA}$ ,  $V_{CCD}$ ,  $V_{CCO}$  may have any value between -0.3 and +5.0 V provided that the supply voltage differences  $\Delta V_{CC}$  are respected.
2. All voltages are typical values and are referenced to all ground pins connected together.

## HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	94	K/W

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## CHARACTERISTICS

$V_{CCA} = V_7$  to  $V_6 = 2.7$  to  $3.6$  V;  $V_{CCD} = V_{10}$  to  $V_9 = 2.7$  to  $3.6$  V;  $V_{CCO} = V_{20}$  to  $V_{19}$  and  $V_{22}$  to  $V_{21} = 2.7$  to  $3.6$  V; AGND, DGND and OGNND shorted together;  $V_{CCA}$  to  $V_{CCD} = -0.15$  to  $+0.15$  V;  $V_{CCD}$  to  $V_{CCO} = -0.15$  to  $+0.15$  V;  $V_{CCA}$  to  $V_{CCO} = -0.15$  to  $+0.15$  V;  $T_{amb} = 0$  to  $70$  °C; typical values measured at  $V_{CCA} = V_{CCD} = V_{CCO} = 3.0$  V and  $T_{amb} = 25$  °C; single-ended input; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_{CCA}$	analog supply voltage		2.7	3.0	3.6	V
$V_{CCD}$	digital supply voltage		2.7	3.0	3.6	V
$V_{CCO}$	output stages supply voltage		2.7	3.0	3.6	V
$I_{CCA}$	analog supply current		32	40	48	mA
$I_{CCD}$	digital supply current		12	16	24	mA
$I_{CCO}$	output stages supply current	ramp input	–	4	6.5	mA
		$f_i = 20$ MHz	–	8.7	12	mA
<b>Internal reference voltage output (pin SDN); note 1</b>						
$V_{ref}$	reference voltage		1.21	1.26	1.31	V
$V_{reg}$	line regulation voltage	$2.7 < V_{CCA} < 3.6$ V	–	1.25	4	mV
TC	temperature coefficient		–	20	–	ppm/K
$I_L$	load current		–1	–	–	mA
<b>Internal reference voltage output (pin REFOUT)</b>						
$V_{ref}$	reference voltage		1.76	1.84	1.92	V
$V_{reg}$	line regulation voltage	$2.7 < V_{CCA} < 3.6$ V	–	1.5	5	mV
TC	temperature coefficient		–	20	–	ppm/K
$I_L$	load current		–1	–	–	mA
<b>Clock input (pin CLK); note 2</b>						
$V_{IL}$	LOW-level input voltage		0	–	0.8	V
$V_{IH}$	HIGH-level input voltage		2	–	$V_{CCD}$	V
$I_{IL}$	LOW-level input current	$V_{CLK} = 0$	–2	–	+2	$\mu$ A
$I_{IH}$	HIGH-level input current	$V_{CLK} = V_{CCD}$	–	–	5	$\mu$ A
$Z_i$	input impedance	$f_{CLK} = 100$ MHz	–	32	–	k $\Omega$
$C_i$	input capacitance	$f_{CLK} = 100$ MHz	–	2	–	pF
<b>Standby input (pin STDBY); see Table 1</b>						
$V_{IL}$	LOW-level input voltage		0	–	0.8	V
$V_{IH}$	HIGH-level input voltage		2	–	$V_{CCD}$	V
$I_{IL}$	LOW-level input current	$V_{STDBY} = 0$	–5	–	–	$\mu$ A
$I_{IH}$	HIGH-level input current	$V_{STDBY} = V_{CCD}$	–	–	5	$\mu$ A
<b>Track enable input (pin <math>\overline{TEN}</math>); see Table 2</b>						
$V_{IL}$	LOW-level input voltage		0	–	0.8	V
$V_{IH}$	HIGH-level input voltage		2	–	$V_{CCD}$	V
$I_{IL}$	LOW-level input current	$V_{TEN} = 0$	–5	–	–	$\mu$ A
$I_{IH}$	HIGH-level input current	$V_{TEN} = V_{CCD}$	–	–	5	$\mu$ A

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Analog inputs (pins INP and INN); input voltage referenced to AGND; <math>V_{REFIN} = 1.27</math> V; see Table 3</b>						
$V_{i(p-p)}$	input voltage range (peak-to-peak value)	$V_i = V_{INP} - V_{INN}$ ; $T_{amb} = 25$ °C	0.90	0.95	1.02	V
$\Delta V_{i(T)}$	input voltage range variation with temperature		–	0.5	–	mV/K
$V_{IO}$	input offset voltage	output code = 127	–30	–	+30	mV
$Z_i$	input impedance	$f_i = 50$ MHz	–	90	–	k $\Omega$
$C_i$	input capacitance	$f_i = 50$ MHz	–	2	–	pF
$I_i$	input current	$V_i = V_{REFOUT} - 0.5$ V	–1	–	–	$\mu$ A
		$V_i = V_{REFOUT} + 0.5$ V	–	–	40	$\mu$ A
<b>Adjustable full-scale range</b>						
$V_{i(p-p)}$	input voltage range (peak-to-peak value)	$V_i = V_{INP} - V_{INN}$ ; $V_{REFIN} = 1.27$ V; $T_{amb} = 25$ °C; see Fig.3	–	1	–	V
<b>Reference input for ADC (pin REFIN); referenced to AGND; note 3</b>						
$V_{REFIN}$	reference input voltage		1.25	1.27	1.35	V
$I_{REFIN}$	reference input current		–	0.9	1.1	mA
<b>ADC data outputs (pins D0 to D7)</b>						
$V_{OL}$	LOW-level output voltage	$I_O = 1$ mA	–	–	0.54	V
		$I_O = 0.6$ mA	–	–	0.40	V
$V_{OH}$	HIGH-level output voltage	$I_O = -0.4$ mA	$V_{CC0} - 0.5$	–	$V_{CC0}$	V
$C_L$	load capacitance		–	–	10	pF
$\delta V/\delta t$	slew rate	20% to 80%; $C_L = 10$ pF	–	1.6	–	V/ns
<b>Analog signal processing; see Figs 4, 5, 6 and 7; note 3</b>						
INL	integral non-linearity	ramp input; $f_{CLK} = 2$ MHz; $V_{CCA} = V_{CCD} = 3$ V	–	$\pm 0.85$	$\pm 1.70$	LSB
DNL	differential non-linearity	ramp input; $f_{CLK} = 2$ MHz; $V_{CCA} = V_{CCD} = 3$ V	–	$\pm 0.25$	$\pm 0.80$	LSB
S/N	signal-to-noise ratio (full-scale)	without harmonics; $f_{CLK} = 100$ MHz:				
		$f_i = 20$ MHz	43	48	–	dB
		$f_i = 50$ MHz	–	47	–	dB
B	–3 dB analog bandwidth	track-and-hold active	–	350	–	MHz
THD	total harmonic distortion	$f_i = 20$ MHz	–	–53	–	dB
		$f_i = 50$ MHz	–	–51	–	dB
$H_{fund(FS)}$	fundamental harmonics (full-scale)	$f_{CLK} = 100$ MHz:				
		$f_i = 20$ MHz	–	–	0	dB
		$f_i = 50$ MHz	–	–	0	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
H <sub>D2(FS)</sub>	second harmonic distortion (full-scale) all components included	differential input; f <sub>CLK</sub> = 100 MHz:				
		f <sub>i</sub> = 20 MHz	–	–63	–	dB
		f <sub>i</sub> = 50 MHz	–	–63	–	dB
		single-ended input; f <sub>CLK</sub> = 100 MHz:				
		f <sub>i</sub> = 20 MHz	–	–57	–	dB
		f <sub>i</sub> = 50 MHz	–	–55	–	dB
H <sub>D3(FS)</sub>	third harmonic distortion (full-scale) all components included	differential input; f <sub>CLK</sub> = 100 MHz:				
		f <sub>i</sub> = 20 MHz	–	–62	–	dB
		f <sub>i</sub> = 50 MHz	–	–55	–	dB
		single-ended input; f <sub>CLK</sub> = 100 MHz:				
		f <sub>i</sub> = 20 MHz	–	–59	–	dB
		f <sub>i</sub> = 50 MHz	–	–55	–	dB
SFDR	spurious free dynamic range	f <sub>CLK</sub> = 100 MHz:				
		f <sub>i</sub> = 20 MHz	–	56	–	dB
		f <sub>i</sub> = 50 MHz	–	54	–	dB
EB	effective number of bits	f <sub>CLK</sub> = 100 MHz; note 4:				
		f <sub>i</sub> = 20 MHz	7.0	7.4	–	bits
		f <sub>i</sub> = 50 MHz	–	7.3	–	bits
		track-and-hold inactive	–	7.4	–	bits
<b>Data timing; f<sub>CLK</sub> = 100 MHz; C<sub>L</sub> = 10 pF; see Fig.8; note 2</b>						
f <sub>CLK(min)</sub>	minimum clock frequency	track-and-hold active	–	–	70	MHz
f <sub>CLK(max)</sub>	maximum clock frequency	I <sub>O</sub> = 0.6 mA	100	–	–	MHz
t <sub>W(CLKH)</sub>	clock pulse width HIGH		4	–	–	ns
t <sub>W(CLKL)</sub>	clock pulse width LOW		4	–	–	ns
t <sub>r</sub>	clock rise time		0.75	–	4	ns
t <sub>f</sub>	clock fall time		0.75	–	4	ns
t <sub>ds</sub>	sampling delay		–	–	1.5	ns
t <sub>h</sub>	output hold time		3	–	–	ns
t <sub>d</sub>	output delay time		–	6	8	ns

## Notes

- The reference output voltage (pin SDN) can be used to drive other analog circuits under the limits indicated.
- In addition to a good layout of the digital and analog grounds, it is recommended that the rise and fall times of the clock must be more than 0.75 ns.
- It is possible with an external reference voltage connected to pin REFIN to adjust the ADC input range. The input range variation will be fixed.
- Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8000 acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (Nyquist frequency). Conversion to signal-to-noise ratio: SINAD = 6.02 × EB + 1.76 dB.



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**Table 1** Standby selection

PIN STDBY	POWER-DOWN MODE	D0 TO D7	I <sub>CCA</sub> + I <sub>CCD</sub>
LOW	inactive	output operating	56 mA
HIGH	active	output logic state LOW	0.7 mA

**Table 2** Track-and-hold selection

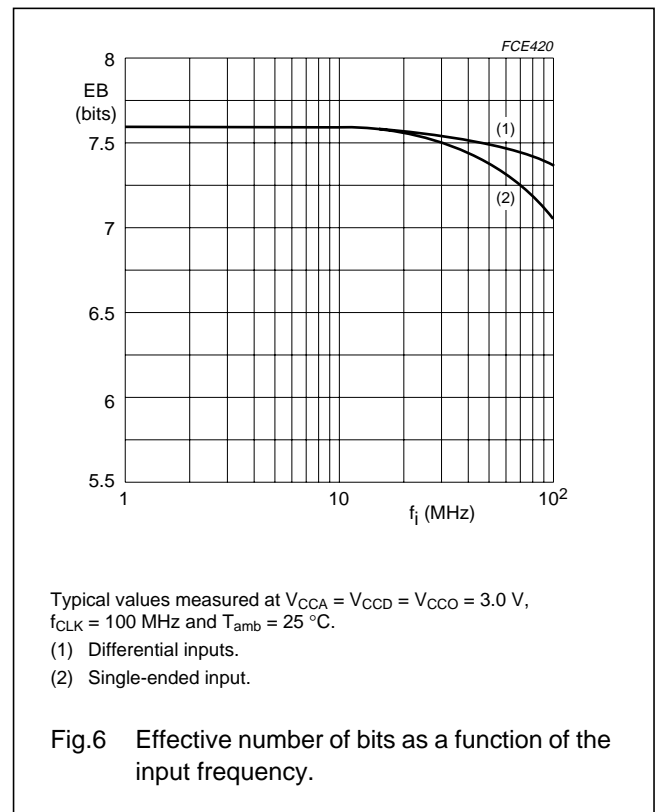
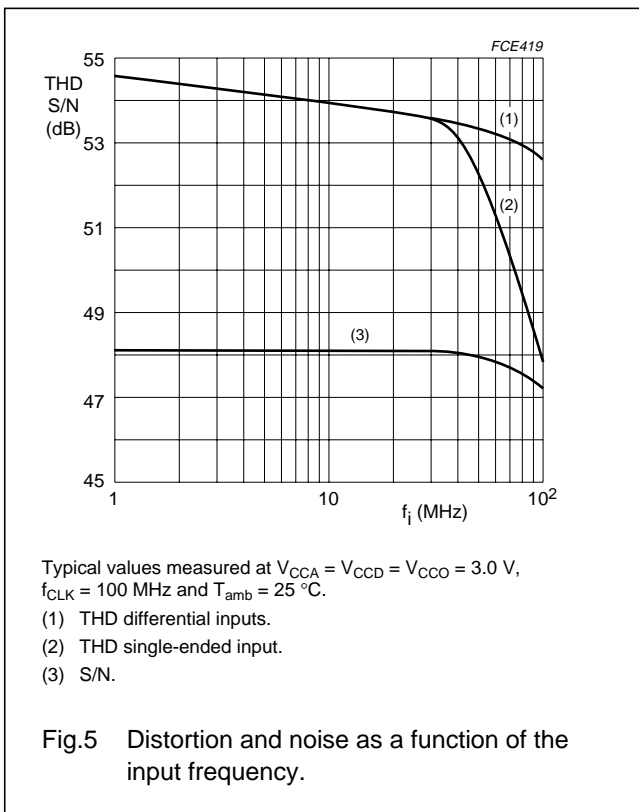
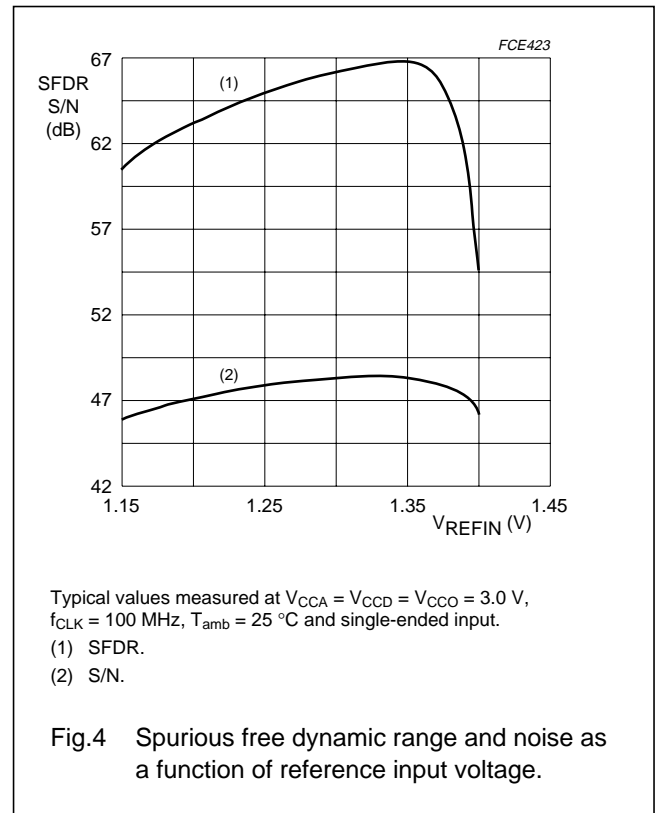
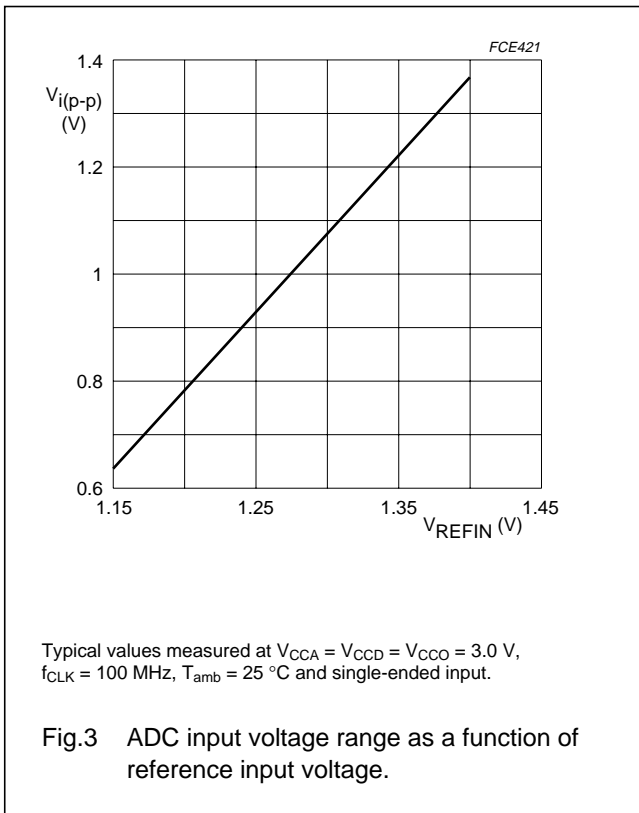
PIN TEN	TRACK-AND-HOLD
LOW	active
HIGH	inactive

**Table 3** Output coding and input voltage (typical values; referenced to AGND; V<sub>REFIN</sub> = 1.27 V)

STEP	V <sub>INP</sub> (V)	V <sub>INN</sub> (V)	OUTPUT CODING BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
Underflow	<1.6	>2.1	0	0	0	0	0	0	0	0
0	1.6	2.1	0	0	0	0	0	0	0	0
1	...	...	0	0	0	0	0	0	0	1
...	...	...	...	...	...	...	...	...	...	...
127	1.85	1.85	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...
254	...	...	1	1	1	1	1	1	1	0
255	2.1	1.6	1	1	1	1	1	1	1	1
Overflow	>2.1	<1.6	1	1	1	1	1	1	1	1

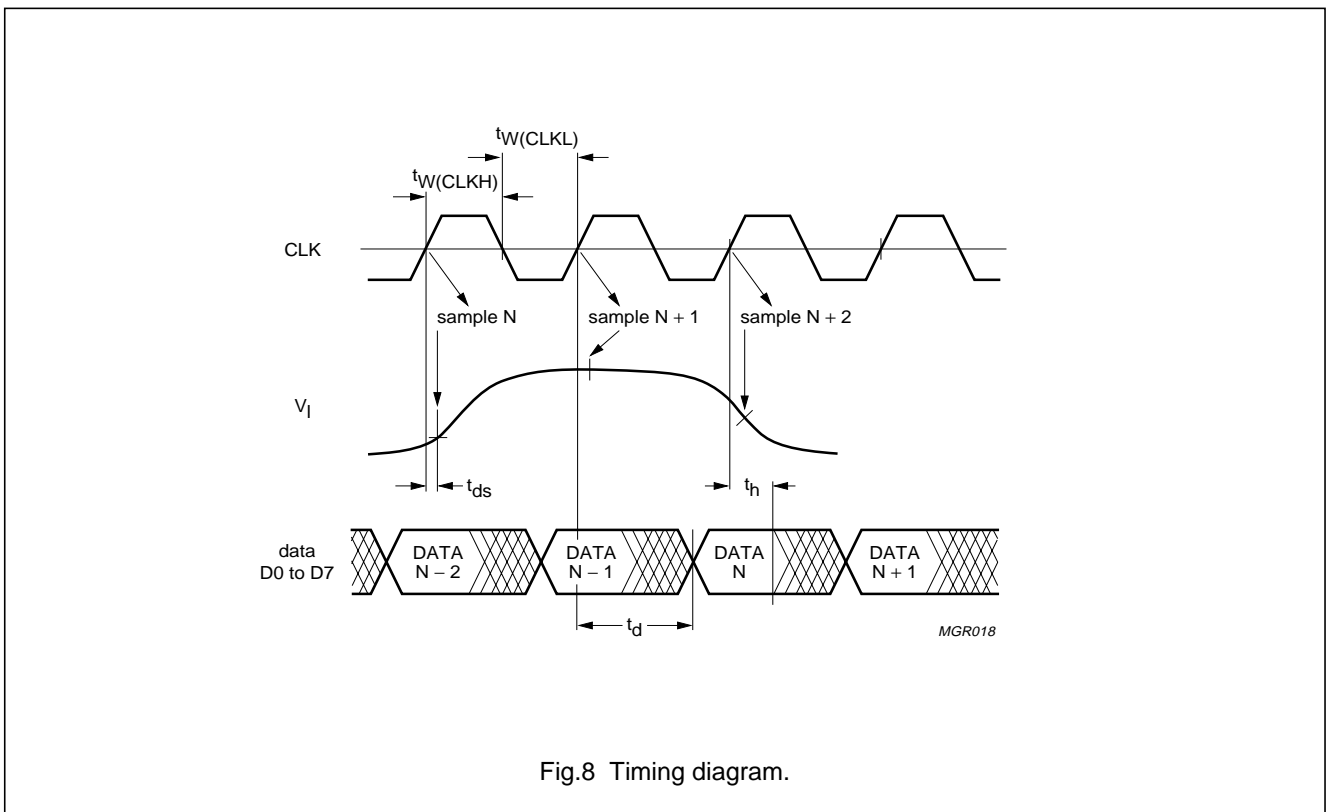
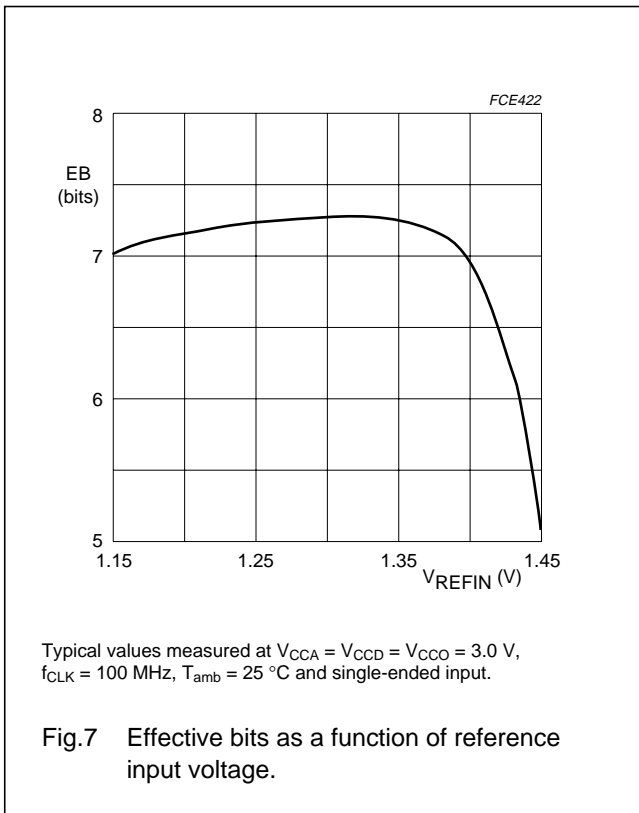
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APPLICATION INFORMATION

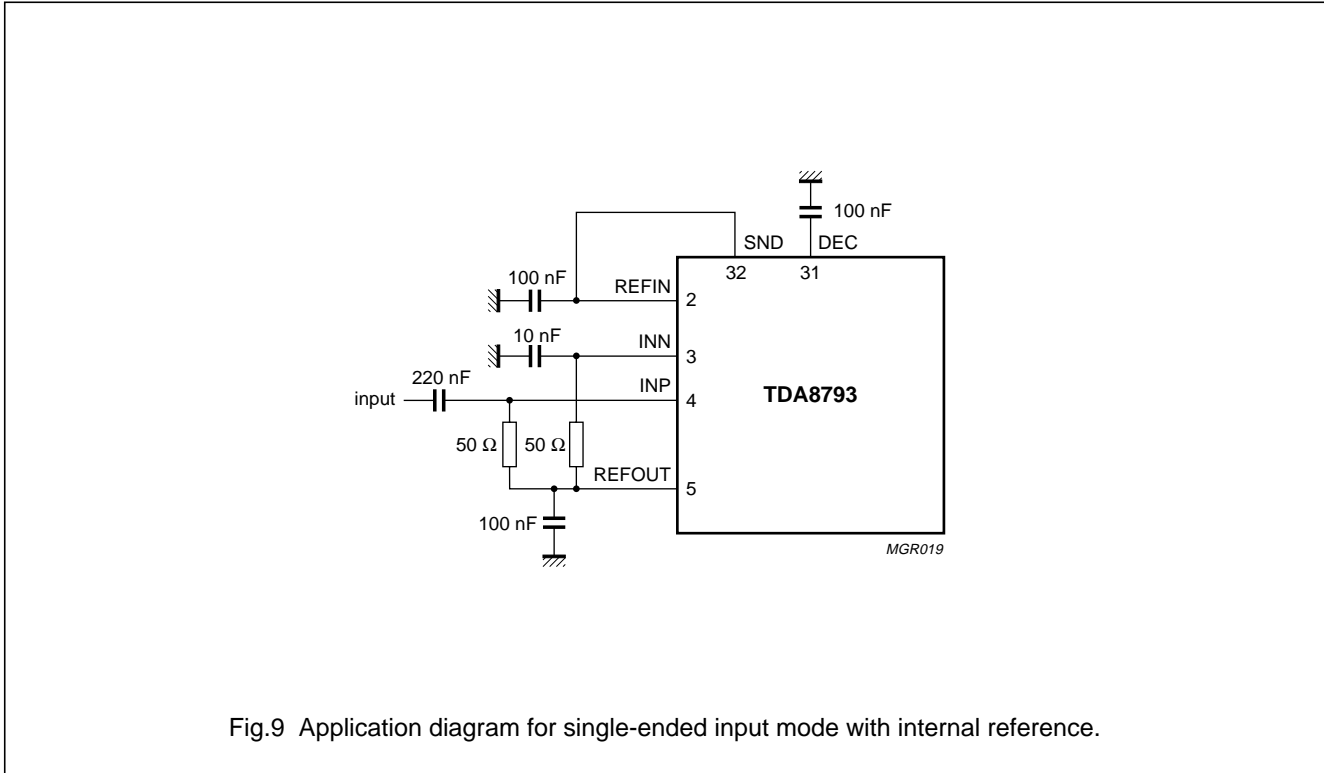


Fig.9 Application diagram for single-ended input mode with internal reference.

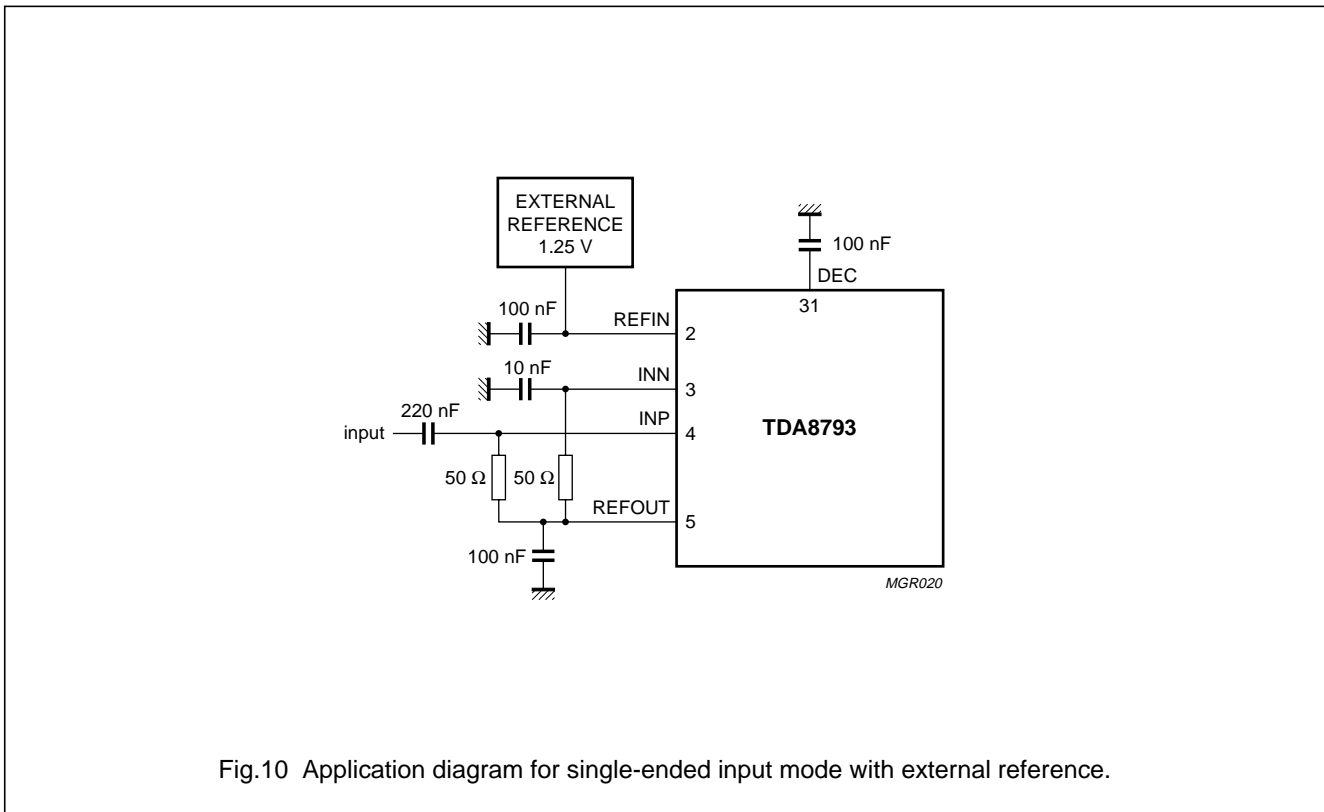


Fig.10 Application diagram for single-ended input mode with external reference.

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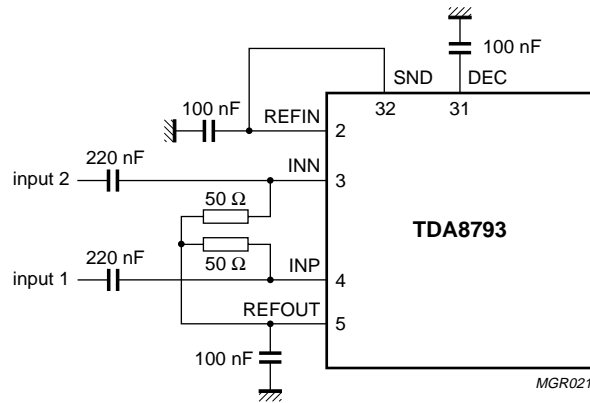


Fig.11 Application diagram for differential input mode with internal reference.

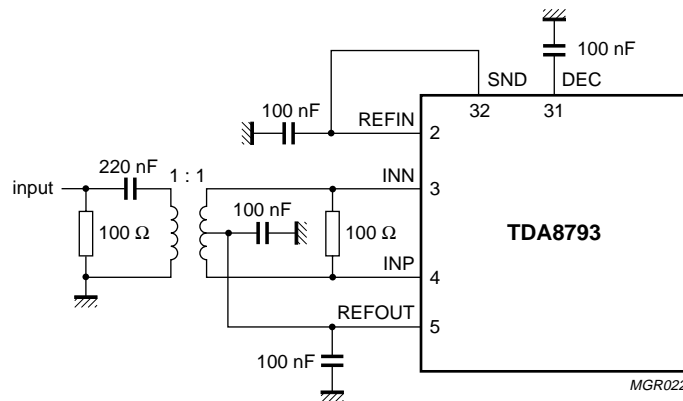


Fig.12 Application diagram for differential input mode with internal reference and using a transformer.

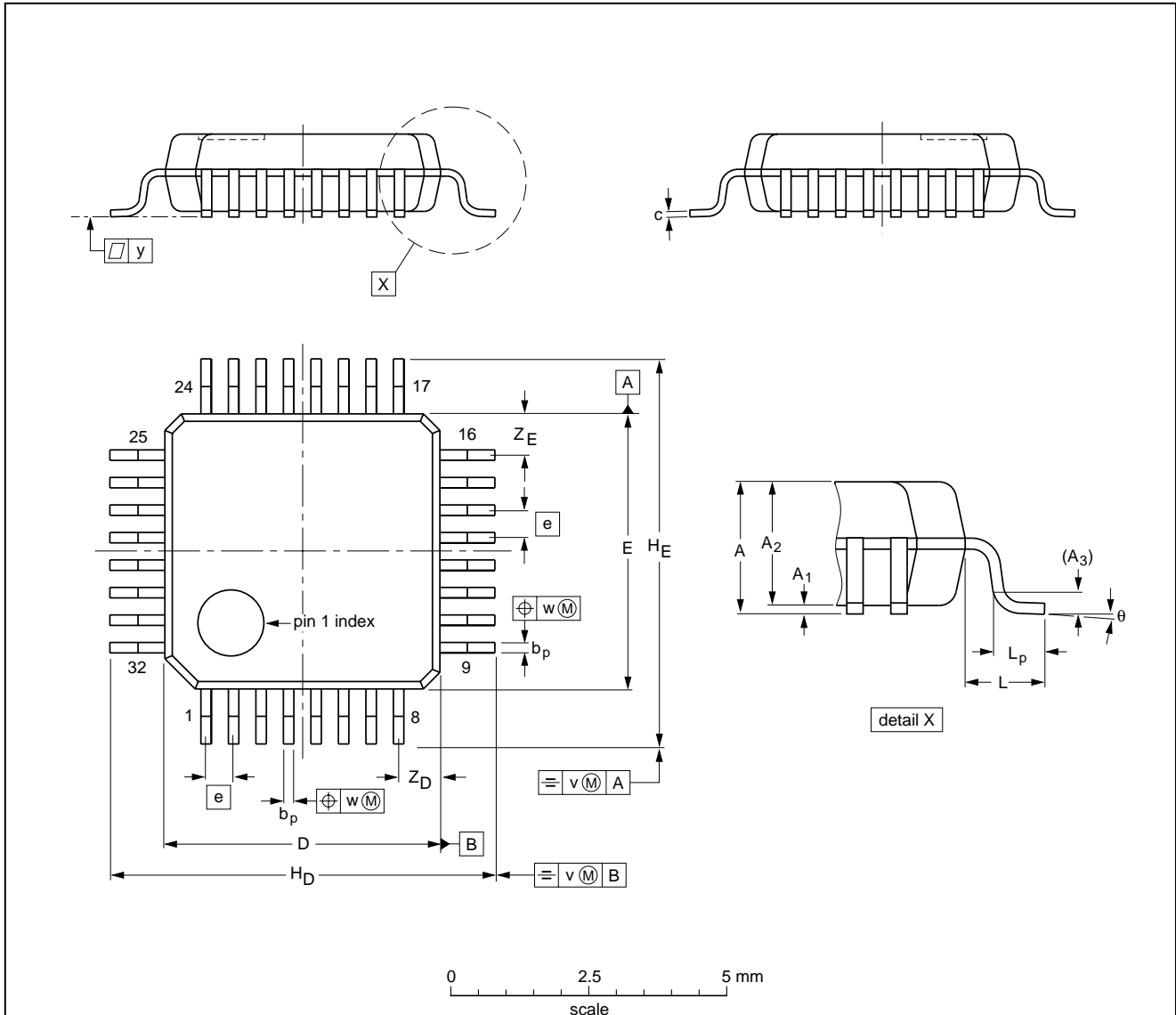
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PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm

SOT401-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note  
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1	136E01	MS-026				99-12-27 00-01-19

## 8-bit, low-power, 3 V, 100 Msps Analog-to-Digital Converter (ADC)

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### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

### Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.



# 8-bit, low-power, 3 V, 100 Msps Analog-to-Digital Converter (ADC)

TDA8793

## DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS <sup>(1)</sup>
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

### Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

## DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Analog-to-Digital Converter (ADC)

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**NOTES**

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**NOTES**

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